Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A magnetic memory cell comprising:

a switching element;

a first magnetic tunnel junction (MTJ) device having a first resistance, the first MTJ device including a first tunnel barrier;

a second MTJ device having a second resistance, the second MTJ device including a second tunnel barrier, wherein the first tunnel barrier has a magneto-resistance (MR) ratio that differs from a MR ratio of the second tunneling barrier; and

a conductor for connecting the first and second MTJ devices in a parallel configuration and for serially connecting the parallel configuration of the first and second MTJ devices to an electrode of the switching element;

wherein the first resistance is different from the second resistance.

2. (Original) The magnetic memory cell of claim 1 wherein the first MTJ device includes a first tunnel barrier that is of a different area than a tunnel barrier of the second MTJ device.

3. (Original) The magnetic memory cell of claim 1 wherein the first MTJ device includes a first tunnel barrier that is of a different thickness than a tunnel barrier of the second MTJ device.

4. (Original) The magnetic memory cell of claim 1 wherein the first MTJ device is a multi-junction MTJ device.

5. (Original) The magnetic memory cell of claim 1 further comprising:

a resistor in series with the second MTJ device;

wherein the second resistance is a combination of a resistance of the second MTJ device and the resistor.

6. (Previously Presented) The magnetic memory cell of claim 1 further comprising:

a conductive member forming at least a portion of one of a bit line and a word line, the portion being connected in series with the second MTJ device;

wherein the second resistance is a combination of a resistance of the second MTJ device and the conductive member.

7. (Cancelled).

8. (Original) The MTJ configuration of claim 1 wherein the first MTJ device includes a synthetic anti-ferromagnetic free layer.

9. (Original) The MTJ configuration of claim 1 wherein the switching element is a transistor.

10. (Original) A magnetic memory cell comprising:

first, second, and third terminals;

a conductor;

a CMOS transistor having source, drain, and gate electrodes, the gate electrode connected to the third terminal, one of either the source or drain connected to the second terminal, and the other of either the source or drain connected to the conductor;

a first magnetic tunnel junction (MTJ) device including a serially connected first free layer, first tunneling barrier, and first pinned layer, the first free layer also being connected to the first terminal and the first pinned layer also being connected to the conductor; and

a second MTJ device including a serially connected second free layer, second tunneling barrier, and second pinned layer, the second free layer also being connected to the first terminal and the second pinned layer also being connected to the conductor;

wherein a first resistance between the first terminal to the second terminal through the first MTJ device is different from a second resistance between the first terminal to the second terminal through the second MTJ device.

11. (Original) The magnetic memory cell of claim 10 wherein the second resistance is twice the first resistance.

12. (Original) The magnetic memory cell of claim 10 wherein the first tunneling barrier is of a

different size than the second tunneling barrier.

13. (Original) The magnetic memory cell of claim 10 wherein the first tunneling barrier is of a different composition than the second tunneling barrier.

14. (Original) The magnetic memory cell of claim 10 wherein the first MTJ device further comprises another free layer, tunneling barrier, and pinned layer serially connected between the first free layer and the first pinned layer.

15. (Original) The magnetic memory cell of claim 14 wherein the first MTJ device is a sandwiched pair of MTJ structures.

16. (Original) The magnetic memory cell of claim 14 wherein the first MTJ device is a serially connected pair of MTJ structures.

17. (Original) The magnetic memory cell of claim 10 further comprising:

a resistor in series with the second MTJ device between the first terminal and the conductor;

wherein the second resistance is a combination of a resistance of the second MTJ device and the resistor.

18. (Original) An integrated circuit comprising:

a plurality of bit lines, word lines, and program lines;

a plurality of magnetic memory cells, each including:

a conductor;

a transistor having source, drain, and gate electrodes, the gate electrode connected to one of the word lines, one of either the source or drain connected to a first program line, and the other of either the source or drain connected to the conductor;

a first magnetic tunnel junction (MTJ) device including a serially connected first free layer, first tunneling barrier, and first pinned layer, the first free layer also being connected to a first bit line and the first pinned layer also being connected to the conductor; and

a second MTJ device including a serially connected second free layer, second tunneling barrier, and second pinned layer, the second free layer also being connected to the first bit line and the second pinned layer also being connected to the conductor;

wherein a first resistance between the first bitline to the conductor through the first MTJ device is different from a second resistance between the first bitline to the conductor through the second MTJ device.

19. (Original) The integrated circuit of claim 18 wherein a first magneto-resistance of the first magnetic junction device is different from a second magneto-resistance of the second magnetic junction device.